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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/829,749	04/10/2001	Roger M. Eddy	FIS920010045US1	9580

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EXAMINER	
DOLE, TIMOTHY J	
ART UNIT	**PAPER NUMBER**
2858	6

DATE MAILED: 12/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/829,749	EDDY ET AL.
	Examiner	Art Unit
	Timothy J. Dole	2858

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-19 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on 26 November 2002 is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. The response to the first office action filed November 26, 2002 is insufficient to overcome the rejection of claims 1-19 as set forth in the last Office action because:

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6, and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. in view of Leedy (USPN 6,288,561).

Referring to claim 1, Lo et al. discloses an electronic circuit test and repair apparatus comprising: at least one wiring analyzer Fig. 1 (40) to locate shorts between conductors (column 5, lines 32-37), a current source Fig. 1 (30), and at least two probes Fig. 1 (14) to contact said conductors in a manner controlled by said wiring analyzer (column 4, lines 58-61).

Lo et al. does not specifically disclose conductors being on a surface of or embedded in a carrier substrate, said conductors being intended to interconnect components to be mounted on said carrier substrate to form a circuit; or a current source to provide a current sufficient to remove shorts.

Leedy discloses conductors being on a surface of or embedded in a carrier substrate, said conductors being intended to interconnect components to be mounted on said carrier substrate to form a circuit (column 3, lines 56-63); and a current source to provide current sufficient to remove shorts (column 6, lines 60-64). It should be noted; Leedy discloses that "high voltage or current" (column 6, line 62) is used in the repair process. Leedy also states that for repairing circuits, the computer can supply appropriate control signals so that "appropriate voltage or current can be applied between the probe points" (column 7, lines 64-67).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to use the conductors on the surface of or embedded in a carrier substrate and current source of Leedy in the apparatus of Lo et al. for the purpose of having the capability to test a variety of products for fault conditions (column 3, lines 56-58) and for removing shorts and repairing electronic circuits since it is stated by Lo et al. that "it is desirable to determine which networks are shorted together, so that the circuit can be repaired" (column 6, lines 54-56).

Referring to claim 2, Lo et al. further discloses a relay wiring analyzer Fig. 1 (40), which is referred to as a processor that accepts a signal from the relays (column 4, lines 47-57) and could therefore be referred to as a relay wiring analyzer.

Lo et al. does not disclose a solid state wiring analyzer.

Leedy discloses an apparatus where the wiring analyzer is a solid state wiring analyzer Fig. 2 (30). It should be noted that Leedy uses active device switching circuitry, such as transistors (column 5, lines 40-42). Therefore the switching could be referred to

as solid state switching and the computer that then analyzes the data could be called a solid state wiring analyzer.

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the solid state wiring analyzer of Leedy into the apparatus of Lo et al. for the purpose of providing two different testing speeds, increasing reliability and reducing the size of the components (column 5, line 49 and column 5, lines 52-54).

Referring to claim 3, Lo et al. as modified discloses the apparatus as claimed except for a controller for automatic positioning of the probes.

Leedy discloses a controller for automatic positioning of the probes (claim 21).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the controller of Leedy into the apparatus of Lo et al. for the purpose of automatically positioning the probes to reduce the possibility of human error or further damage due to additional handling.

Referring to claim 4, Lo et al. discloses the apparatus as claimed where the probes comprise a cluster probe (column 4, lines 39-41). It should be noted that a cluster probe comprises a set of test probes that all simultaneously contact the device under test. Therefore, according to column 1, lines 17-19, the probing device as disclosed by Lo et al. could be called a cluster probe.

Referring to claim 5, Lo et al. discloses the test and repair apparatus as claimed except for a controller having voltage stress test capability.

Leedy et al. discloses a controller having voltage stress test capability. It should be noted, Leedy states that a computer can provide control signals to the probes so that

high voltage can be provided between the appropriate probe points (column 6, lines 60-63), which could be considered a controller for voltage stress testing.

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the controller of Leedy into the apparatus of Lo et al. for the purpose of having voltage stress test capability, since it is useful in testing, to make sure a repaired short does not regenerate and to avoid further faults.

Referring to claim 6, Lo et al. discloses the apparatus as claimed except for a controller to automate at least one of locating circuit shorts and removing circuit shorts.

Leedy discloses a controller to automate at least one of locating circuit shorts and removing circuit shorts (claim 6 (b) and (d)).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the controller of Leedy into the apparatus of Lo et al. for the same purpose as given in claim 3, above.

Referring to claim 14, Lo et al. discloses an apparatus for test and repair of wiring interconnect packages, comprising: at least one wiring analyzer Fig. 1 (40) to locate circuit shorts, a current source Fig. 1 (30), and a cluster probe (column 4, lines 39-41). It should be noted that the probing device as disclosed by Lo et al. could be called a cluster probe as shown in claim 4, above.

Lo et al. does not disclose that the test and repair apparatus is able to provide a current sufficient to remove shorts.

Leedy discloses a current source to provide current sufficient to remove shorts (column 6, lines 60-64).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to use the current source of Leedy in the apparatus of Lo et al. for the same purpose as given in claim 1, above.

Referring to claim 15, Lo et al. further discloses a relay wiring analyzer Fig. 1 (40), which is a processor that could be referred to as a relay wiring analyzer as shown in claim 2, above.

Lo et al. does not disclose a solid state wiring analyzer.

Leedy discloses an apparatus where the wiring analyzer is a solid state wiring analyzer Fig. 2 (30). It should be noted that Leedy uses a computer to analyze data from active device switching circuitry, which could be referred to as a solid state wiring analyzer as shown in claim 2, above.

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the solid state wiring analyzer of Leedy into the apparatus of Lo et al. for the same purpose as given in claim 2, above.

Referring to claim 16, Lo et al. as modified discloses the apparatus as claimed except for a controller to automatically position the cluster probe.

Leedy discloses a controller for automatic positioning the cluster probe (claim 21).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the controller of Leedy into the apparatus of Lo et al. for the same purpose as given in claim 3, above.

Referring to claim 17, Lo et al. discloses the test and repair apparatus as claimed except for a controller having voltage stress test capability.

Leedy et al. discloses a controller having voltage stress test capability. It should be noted that the computer disclosed by Leedy could be considered a controller for voltage stress testing as shown in claim 5, above.

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the controller of Leedy into the apparatus of Lo et al. for the same purpose as given in claim 5, above.

Referring to claim 18, Lo et al. discloses the apparatus as claimed except for a controller so that at least one of locating circuit shorts and removing circuit shorts is animated.

Leedy discloses a controller to automate at least one of locating circuit shorts and removing circuit shorts (claim 6 (b) and (d)).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the controller of Leedy into the apparatus of Lo et al. for the same purpose as given in claim 3, above.

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. as applied to claim 1 above, and further in view of Kerschner.

Lo et al. as modified discloses the test and repair apparatus as claimed except the wiring analyzer does not additionally locate open circuits.

Kerschner discloses a wiring analyzer that locates open circuits (column 4, lines 19-39).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the wiring analyzer of Kerschner into the test and repair apparatus of Lo et al. for the purpose of locating open circuits since further fault detection is useful in determining the quality of a device under test.

5. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. as applied to claim 6 above, and further in view of Craig et al.

Lo et al. discloses the test and repair apparatus as claimed except he does not disclose that the controller performs a plurality of attempts to remove the shorts.

Craig et al. discloses a plurality of attempts to remove the shorts (claim 4 (2)).

Therefore it would have been obvious to one skilled in the art at the time of the invention to incorporate a plurality of attempts as shown by Craig et al. in the apparatus of Leedy for the purpose of removing shorts (column 8, lines 39-55).

6. Claims 9-13 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. in view of Leedy (USPN 6,288,561), and further in view of Kerschner.

Referring to claim 9, Lo et al. discloses a method of testing wiring interconnect packages comprising: contacting a predetermined set of locations on a wiring interconnect package using a cluster probe containing a plurality of probes (claim 1): applying a predetermined set of voltages in a predetermined sequence to predetermined

probes in the cluster probe (claim 1); and measuring a response to each application of voltages to detect any short circuits in the wiring interconnect package (claim 1).

Lo et al. does not disclose that open circuits will be detected, or that for any detected short circuits, a predetermined voltage will be applied to attempt to remove the detected short circuits, where the applying of voltages and measuring of responses to detect any short circuits uses the same apparatus that would be used for attempting to remove the short circuits.

Kerschner discloses a method to detect open circuits (column 4, lines 19-39).

Leedy discloses a test and repair method where for any detected short circuits, a predetermined voltage is applied to attempt to remove the detected short circuits (column 6, lines 55-58), where the applying of voltages and measuring of responses to detect any short circuits uses the same apparatus that is used for attempting to remove the short circuits (column 7, lines 10-15).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the method of open circuit detection of Kerschner and the repair method of Leedy into the method of Lo et al. for the purpose of detecting open circuits, since further fault detection is useful in determining the quality of a device under test, and repairing short circuits since it is stated by Lo et al. that "it is desirable to determine which networks are shorted together, so that the circuit can be repaired" (column 6, lines 54-56).

Referring to claim 10, Lo et al. discloses the method as claimed except for automating one of the following: the contacting at a predetermined set of locations; the

detecting of abnormal open and short circuits: and the attempting to remove the short circuits.

Leedy discloses a method where at least one of the following is automated: the contacting at a predetermined set of locations; the detecting of abnormal open and short circuits: and the attempting to remove the short circuits (Leedy: column 6, lines 28-58).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the method of Leedy into the method of Lo et al. for the purpose of automatically contacting locations, detecting open circuits and short circuits, and/or attempting to remove short circuits since it would reduce the possibility of human error or further damage due to additional handling.

Referring to claim 11, Lo et al. discloses a method of automatically testing wiring interconnect packages comprising: contacting a predetermined set of locations on a wiring interconnect package using a cluster probe containing a plurality of probes (claim 1); automatically applying a predetermined set of voltages in a predetermined sequence to predetermined probes in the cluster probe (claim 1); and automatically measuring a response to each application of voltages to detect any short circuits in the wiring interconnect package (claim 1). It should be noted that the processor of Lo et al. controls the whole testing process (column 4, lines 58-61).

Lo et al. does not disclose that open circuits will be detected, or that for any detected short circuits, a predetermined voltage will be automatically applied to attempt to remove the detected short circuits.

Kerschner discloses a method to detect open circuits (column 4, lines 19-39).

Leedy discloses a test and repair method where for any detected short circuits; a predetermined voltage is automatically applied to attempt to remove the detected short circuits (column 6, lines 55-58).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the method of open circuit detection of Kerschner and the repair method of Leedy into the method of Lo et al. for the same purpose as given in claim 9, above.

Referring to claim 12, Lo et al. discloses a relay switching module Fig 1 (42) for controlling the relays.

Lo et al. does not disclose that the detecting of opens or shorts is executed at a first higher speed using a solid state switching module or that the relay switching module is used to attempt to remove shorts.

Leedy discloses that testing is executed at a first higher speed using a solid state switching module Fig 2 (50), (column 5, lines 40-42 and 46-48). It should be noted that Leedy uses a computer to analyze data from active device switching circuitry, which could be referred to as a solid state wiring analyzer as shown in claim 2, above. Leedy also discloses an attempt to remove shorts (column 6, lines 60-64).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the solid state switching module and repair method of Leedy into the method of Lo et al. for the purpose of detecting opens or shorts at a higher speed, increasing reliability, reducing the size of components and attempting to remove shorts

using relays, since relays are more durable than transistors in that they can handle a larger current or voltage spike used for repairing short circuits.

Referring to claim 13, Lo et al. discloses the method as claimed except for automating the contacting of the wiring interconnect package.

Leedy discloses a method where contacting the wiring interconnect package is additionally automatically actuated by a controller (column 6, lines 28-39).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the method of Leedy into the method of Lo et al. for the purpose of automatically contacting the wiring interconnect package since it would reduce the possibility of human error or further damage due to additional handling.

Referring to claim 19, Lo et al. discloses a signal-bearing medium tangibly embodying a program of machine-readable instructions executable by a digital processing apparatus to perform a method of testing wiring interconnect packages (column 4, line 61 – column 5, line 5), comprising: contacting a predetermined set of locations on a wiring interconnect package using a cluster probe containing a plurality of probes (claim 1); applying a predetermined set of voltages in a predetermined sequence to predetermined probes in the cluster probe (claim 1); and measuring a response to each application of voltages to detect any short circuits in the wiring interconnect package (claim 1).

Lo et al. does not disclose that open circuits will be detected, or that for any detected short circuits, a predetermined voltage will be applied to attempt to remove the detected short circuits, where the applying of voltages and measuring of responses to

detect any short circuits uses the same apparatus that would be used for attempting to remove the short circuits.

Kerschner discloses a method to detect open circuits (column 4, lines 19-39). Leedy discloses a test and repair method where for any detected short circuits, a predetermined voltage is applied to attempt to remove the detected short circuits (column 6, lines 55-58), where the applying of voltages and measuring of responses to detect any short circuits uses the same apparatus that is used for attempting to remove the short circuits (column 7, lines 10-15).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the method of open circuit detection of Kerschner and the repair method of Leedy into the method of Lo et al. for the same purpose as given in claim 9, above.

Response to Arguments

7. Applicant's arguments filed November 26, 2002 have been fully considered but they are not persuasive.

8. In response to the Applicants argument that the Examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the

applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

The combination of Leedy into Lo et al. is considered to be appropriate since the Leedy reference refers to a method and apparatus to perform testing and repair of integrated circuits. Since integrated circuits are types of electronic circuits, the Leedy reference is fully applicable to claim 1.

9. In response to the Applicants argument that the Leedy reference would not have sufficient energy to repair the short circuit defects on printed circuit boards, the Applicants are relying on facts not stated in the claims. Now, if there were some special **structural and/or functional** reasons for the claimed shape that renders the claim patentably distinct over prior art, **then these have to be clear from the claim itself**. It should be emphasized that to establish any such distinction; the Applicants cannot rely on the specification. That is, they **cannot** rely on factors not recited in the rejected claim. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). See also *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1571-72 7 USPQ2d 1057, 1064-1065 (Fed. Cir.), *cert denied*, 488 U.S. 892 (1988), in which it was held that various limitations on which the appellant relied could not be given meaning since they **were not stated in the claims.** In *Ex parte McCullough*, 7 USPQ2d 1889, 1891 (Bd. Pat. App. & Inter. 1987), a claimed electrode was rejected although it was asserted in the **specification** that it functions differently from prior art electrodes, since

"although the demonstrated results may be germane to the patentability of a battery containing appellant's electrode, they are not germane to the invention claimed on appeal."

10. In response to the Applicants argument that there is no teaching of "... at least one wiring analyzer to locate shorts between conductors on a surface of a carrier substrate, said conductors intended to interconnect components to be mounted on said carrier substrate to form a circuit; a current source to provide current sufficient to remove said shorts..." (page 4, paragraph 3); please refer back to the rejection stated on page three of this office action wherein Leedy teaches the limitation as claimed.

11. In response to the Applicants argument that neither Leedy nor any of the other references make any suggestion of a second analyzer and therefore it is improper to combine the Leedy reference with that of Lo et al. for the purpose of having a second analyzer whereby allowing testing at a two different speeds. It should be noted, Leedy states that by using active device switching circuitry, or solid state switching, "higher at-speed tests can be performed" (column 5, line 49). Leedy goes on to state that it is desirable to additionally use active device switching since "The incorporation of active device switching circuitry into probing devices would create intelligent and programmable probing devices" (column 5, lines 52-54).

12. The Applicants finally argue that none of the references cited are applicable to claims 5 and 17. It should be emphasized that "apparatus claims must be structurally distinguishable from the prior art." MPEP 2114. In *In re Danly*, 263 F. 2d 844, 847, 120 USPQ 528, 531 (CCPA

1959) it was held that apparatus claims must be distinguished from prior art in terms of **structure** rather than **function**. In *Hewlett-Packard Co v Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990), the court held that: "Apparatus claims cover what a device **is**, not what it **does**." (emphases in original). To emphasize the point further, the court added: "An invention need not **operate** differently than the prior art to be patentable, but need only **be** different" (emphases in original).

That is, in an apparatus claim, if a prior art structure discloses all of the **structural elements** in the claim, as well as their relative juxtaposition, then it **reads** on the claim, regardless of whether or not the **function** for which the prior art structure was intended is the same as that of the claimed invention.

Therefore, referring to apparatus claims 5 and 17, a **controller** is claimed. It should be noted that according to the claim rejections, Leedy shows a computer can provide control signals to the probes so that high voltage can be provided between the appropriate probe points (column 6, lines 60-63). Therefore, the computer could be considered a controller.

Final Rejection

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Timothy J. Dole whose telephone number is 703-305-7396. The examiner can normally be reached on Mon. thru Fri. from 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, N. Le can be reached on 703-308-0750. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-1782.

TJD
December 16, 2002

Tim J. Dole

N. Le
Supervisory Patent Examiner
Technology Center 2800